IN THE CLAIMS

Please accept amended claims 1 and 16 as follows:

1. (currently amended) A one-time programmable memory device, comprising:

an isolation layer for defining an active area of a substrate;

an oxide layer formed on the active area;

a floating gate formed over the active area and the isolation layer;

an inter-gate dielectric layer formed on the floating gate; and

a control gate formed on the inter-gate dielectric layer, wherein a first portion of the floating gate formed over the active area is narrower than a second portion of the floating gate formed over the isolation layer, and wherein the control gate is formed over the second portion of the floating gate and not over the first portion of the floating gate, and wherein a plurality of edges of the control gate are formed to be within corresponding edges of the floating gate such that an area of the isolation layer ~~covered~~ overlapped by the second portion is greater than an area of the isolation layer ~~covered~~ overlapped by the control gate.

2. (previously presented) The one-time programmable memory device of claim 1, further comprising a source region and a drain region formed in the active area at least one of under or adjacent both sides of the floating gate.

3. - 5. (canceled)

6. (original) The one-time programmable memory device of claim 1, wherein the inter-gate dielectric layer includes a silicon nitride layer.

7. (original) The one-time programmable memory device of claim 6, wherein the inter-gate dielectric layer includes a composite layer having a silicon oxide layer and a silicon nitride layer.

8. (original) The one-time programmable memory device of claim 6, wherein the inter-gate dielectric layer includes a composite layer having a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer.

9. – 15. (canceled)

16. (currently amended) An integrated circuit, comprising:

a plurality of isolation layers for defining a first area, a second area, and a third area in a substrate;

a memory device including a floating gate formed over the first area and at least one isolation layer of the plurality of isolation layers, an inter-gate dielectric layer formed on the floating gate and including a composite layer having a silicon oxide layer and a silicon nitride layer, and a control gate formed on the inter-gate dielectric layer;

a first transistor including a first gate formed of the same material as the control gate, wherein the first gate is formed in the second area of the substrate on a

first gate oxide layer having a thickness greater than or equal to a thickness of a tunnel oxide layer formed on the substrate, and a first source region and a first drain region formed in the second area at least one of under or adjacent both sides of the first gate; and

a second transistor including a second gate formed of the same material as the control gate, wherein the second gate is formed in the third area of the substrate on a second gate oxide layer thinner than the first gate oxide layer, and a second source region and a second drain region formed in the third area at least one of under or adjacent both sides of the second gate, wherein a first portion of the floating gate formed over the first area is narrower than a second portion of the floating gate formed over the at least one isolation layer, and wherein the control gate is formed over the second portion of the floating gate and not over the first portion of the floating gate, and a plurality of edges of the control gate do not extend to corresponding edges of the floating gate.

17.-23. (canceled)

24. (previously presented) An integrated circuit, comprising:

a memory device including an isolation layer for defining an active area of a substrate, a tunnel oxide layer formed on the active area, a floating gate formed over the active area and the isolation layer, an inter-gate dielectric layer formed on the floating gate, and a control gate formed on the inter-gate dielectric layer;

a first transistor including a first gate, a first gate oxide layer interposed

between the first gate and the substrate, and a first source region and a first drain region formed in the active area at least one of under or adjacent both sides of the first gate; and

a second transistor including a second gate, a second gate oxide layer interposed between the second gate and the substrate, and a second source region and a second drain region formed in the active area at least one of under or adjacent both sides of the second gate, wherein the second gate oxide layer is thinner than the tunnel oxide layer, and the first gate oxide layer is thicker than the tunnel oxide layer and the second gate oxide layer.

25. (previously presented) The integrated circuit of claim 24, wherein the memory device further includes a source region and a drain region formed in the active area at least one of under or adjacent both sides of the floating gate.

26. (previously presented) The integrated circuit of claim 24, wherein the first gate and the second gate are formed of the same material as the control gate.